Intel® 440MX Entry PrPMC Platform

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Revision History

CAD REV.	SCH REV.	DESCRIPTION
X0.0	X1.0	Initial artwork release (No artwork generated)
X2.0	X2.0	Connectors, Jn3 and Jn4 were reversed, new artwork required.
X2.0	X2.1	RESISTORS R83,R84,R87,R88 HAD WRONG PART NUMBERS.

Title: Title Page

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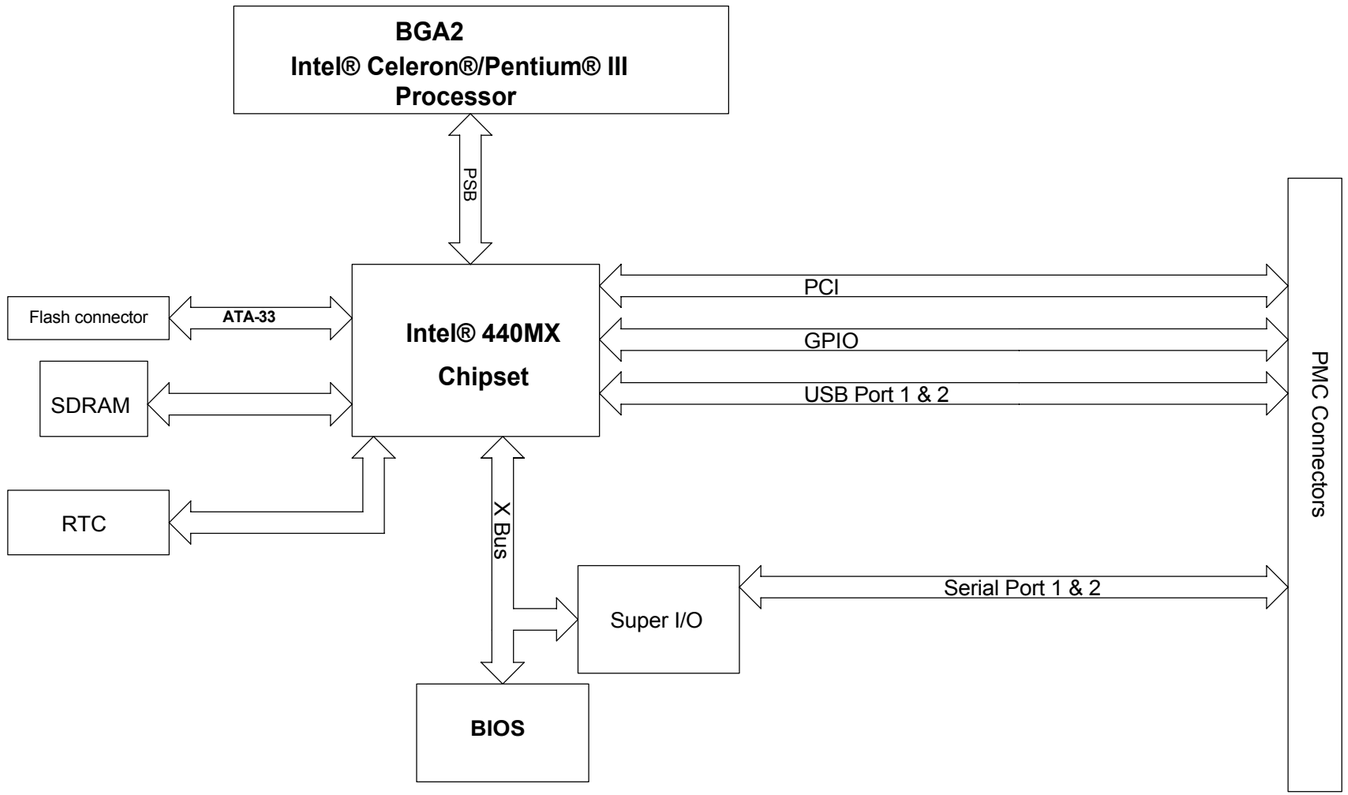
Block Diagram



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General Board Design Requirements

>> PWB must be routed using ten (10) layers, with the following stackup:

	Layer 1 Top	(.7)		Layer 1 Top	(.7)
	4 mil			4 mil	
(1.4)	Layer 2 Plane (GND)		(1.4)	Layer 2 Plane (GND)	
	7 mil			4 mil	
	Layer 3 Signal	(.7)		Layer 3 Signal	(.7)
	7 mil			12 mil	
(1.4)	Layer 4 Plane (GND)		(.7)	Layer 4 Signal	
	4 mil			4 mil	
	Layer 5 Plane (Power)	(1.4)		Layer 5 Plane Power	(1.4)
	4 mil		Alternate	4 mil	
(1.4)	Layer 6 Plane (Power)			Layer 6 Plane (GND)	(1.4)
	4 mil			4 mil	
	Layer 7 Plane (GND)	(1.4)	(.7)	Layer 7 Signal	
	7 mil			12 mil	
	Layer 8 Signal	(.7)		Layer 8 Signal	(.7)
(1.4)	7 mil			4 mil	
	Layer 9 Plane (GND)			Layer 9 Plane (GND)	(1.4)
	4 mil			4 mil	
	Layer 10 Bottom			Layer 10 Bottom	(.7)
		(.7)			

>> Size **59.2 mils** **61.1 mils**

>> Right angle traces must not be used.

>> Vias for decoupling capacitors must be kept as close as possible to the capacitor pad.

>> Trace impedance must be 56 ohms, +-10%

>> Total board thickness must be .062" +0%, -20%

>> Board material must be FR-4.

>> GND layers must not be split.

>> Top and bottom (outer) layers must be no less than 1/2 oz copper before plating, inner layers must be 1 oz copper.

>> Series terminating resistors must be kept as close to the driving pin as possible.

>> Daisy chain signals going to more that on point, do not use stubs.

>> Unless otherwise noted, all signal traces should be no less than 4 with a preferred 5 mil width.

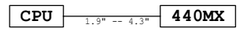
>> Unless otherwise noted, minimum space between traces is 5 mils, including adjacent layers. This is only for parallelisms of greater than .25", vias are exempt from this rule.

>> Specific routing reqirements may be included throughout schematic sheets.

>> One registration target must be included on each corner of the board.

CPU Routing Requirements

>> Route all GTL traces between CPU and 440MX as shown in the diagram to the right.



>> Route all traces between CPU and 440MX on a layer adjacent to a ground plane without multiple layer changes.

>> All traces between CPU and 440MX should differ in length by no more than 1000 mils.

>> Minimum space between traces is 5 mils (unless otherwise noted), this includes adjacent signal layers.

>> Minimum space between traces may be reduced to 4 mils when breaking out of a footprint. The total length of trace routed using 4 mil spacing must be less than 250 mils. This refers to groups listed below.

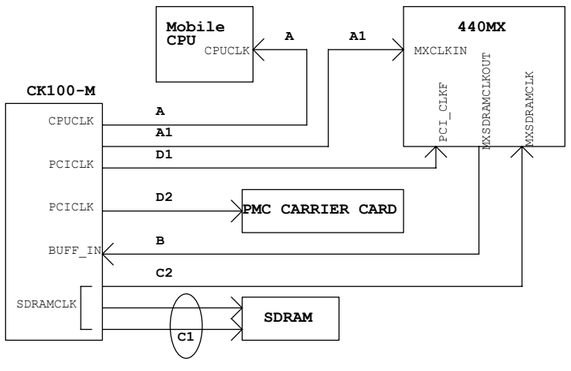
>> The following signals are shown in groups seperated by commas each group requires 25 mil spacing from other groups, including adjacent layers.

-A[3..31], -D[0..63], -ADS, -HTRDY, -HREQ[0..4], [-BREQ0, -BNR, -BPRI, -HLOCK, -DEFER, -DBSY, -DRDY,-HIT, -HITM,], [-A20M, -FLUSH, -IGNNE, -INIT,INTR,NMI, PWRGDCPU, -SMI,-SLEEP, -STPCLK,-FERR, -CPURST], -RS[0..2], THERMD[P:N], PLL[1:2], [TCK,TMS,TDI, TDO, -TRST,-PRDY, -PREQ].

>> Route THERMDA and THERMDC close together as a pair (no more than 250 mil difference in length), on same layer, in parallel, and 25 mils min from any other trace.

>> Route PLL[1:2] using 25 mil minimum width trace, minimize loop area, and separate from all other traces by 25 mils minimum. Preferably a plane on the component side of the PWB would be used.

Clock Specific Routing Requirements



Variable	Trace Length(min)	Trace Length(max)	Trace Width
A	2"	4.5"	5 mil
A1	A+1.25"	A+1.35"	5 mil
B	0"	4.5"	5 mil
C1	0"	4.5"	5 mil
C2	C1+2.4 inches	C1+2.6 inches	5 mil
D1	A1+7"	A1+10"	5 mil
D2	A1	A1+1"	5 mil

Memory Bus Specific Routing Requirements

>> Minimum trace width is 4 mils.

>> Minimum space between memory trace groups is 10 mils, this includes adjacent signal layers.

>> Minimum space between memory traces and other non-memory groups is 25 mils, this includes adjacent signal layers.

>> Memory address, data, and control lines must be routed as separate groups and treated as different signal types.

>> The MD, DQM, -CS, CKE, -SRAS, -SCAS, -SWE, and MA signals (between MX and MEMORY) must be between 1" and 6" in length, matched to within 600 mils.

Memory Bus GROUPS -- MEMORY Names

>> Address Signals: MA[0..11]

>> Address Signals: BA[0:1]

>> Data Signals: MD[0..63]

>> Control Signals:

CKE[0:1], SDA, SCL, -CS[0:1], -SWE, -SCAS, -SRAS

PCI Bus Specific Routing Requirements

>> The 440MX must be the last device on the PCI bus.

>> PCI bus max length must be less than 6".

PCI Bus GROUPS

>> Address/Data Signals: AD[0..31]

>> Control Signals:

-CBE[0..3], -REQ[0..3], -GRNT[0..3], -PIRQ[A:D], -PCIRST, -FRAME, -TRDY, -IRDY, -STOP, -DEVSEL, -SERR, -PERR, PAR, -PLOCK

Power Supply Specific Routing Requirements

>> All unrelated signals and power planes must be kept away from the switching circuits.

>> All traces associated with the input power/ground connectors, and the capacitors connected to these connectors, must be routed with minimum length and maximum width.

>> See the Power Supply schematic sheet for complete restrictions.

IDE Specific Routing Requirements

>> Place IDE conector within 3" of 440MX.

>> Place IDE series terminating resistors within 500 mils of the 440MX.

USB Specific Routing Requirements

>> USB signals should maintain a Z of 45 ohms +-5%.

General Notes

>> Signals prefixed with an "-" are low active.

>> Signals suffix of an "-", "+" indicate minus and plus of differential pairs.

Title	Routing Guidelines	
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Height = .100

RN1A
1.5K

U1A
Intel
Celeron/Pentium III BGA2

10	-A20M	-A20M	-A20M	AD10	A20M		
7	-D[0..63]	-D[0..63]	-D0	D10	D0		
			-D1	D11	D1		
			-D2	C7	D2		
			-D3	C8	D3		
			-D4	B9	D4		
			-D5	A9	D5		
			-D6	C10	D6		
			-D7	B11	D7		
			-D8	C12	D8		
			-D9	B13	D9		
			-D10	A14	D10		
			-D11	B12	D11		
			-D12	E12	D12		
			-D13	B16	D13		
			-D14	A13	D14		
			-D15	D13	D15		
			-D16	D15	D16		
			-D17	D12	D17		
			-D18	B14	D18		
			-D19	E14	D19		
			-D20	C13	D20		
			-D21	A19	D21		
			-D22	B17	D22		
			-D23	A18	D23		
			-D24	C17	D24		
			-D25	D17	D25		
			-D26	C18	D26		
			-D27	B19	D27		
			-D28	D18	D28		
			-D29	B20	D29		
			-D30	A20	D30		
			-D31	B21	D31		
			-D32	D19	D32		
			-D33	C21	D33		
			-D34	E18	D34		
			-D35	C20	D35		
			-D36	F19	D36		
			-D37	D20	D37		
			-D38	D21	D38		
			-D39	H18	D39		
			-D40	F18	D40		
			-D41	J18	D41		
			-D42	E21	D42		
			-D43	E20	D43		
			-D44	H19	D44		
			-D45	E21	D45		
			-D46	J20	D46		
			-D47	H21	D47		
			-D48	L18	D48		
			-D49	G20	D49		
			-D50	P18	D50		
			-D51	G21	D51		
			-D52	K18	D52		
			-D53	K21	D53		
			-D54	M18	D54		
			-D55	L21	D55		
			-D56	R19	D56		
			-D57	K19	D57		
			-D58	T20	D58		
			-D59	J21	D59		
			-D60	L20	D60		
			-D61	M19	D61		
			-D62	U18	D62		
			-D63	R18	D63		
			TP16 -DEP0	V20	DEP0		
			TP17 -DEP1	T21	DEP1		
			TP18 -DEP2	U21	DEP2		
			TP19 -DEP3	R21	DEP3		
			TP20 -DEP4	V18	DEP4		
			TP21 -DEP5	P21	DEP5		
			TP22 -DEP6	P20	DEP6		
			TP23 -DEP7	U19	DEP7		
13	CPUCLK	CPUCLK	CPUCLK	M3	BCLK		
10	-STPCLK	-STPCLK	-STPCLK	AC11	STPCLK		
6	-LOCK	-LOCK	-LOCK	R1	LOCK		
			-FLUSH	AC9	FLUSH		
6	-HTRDY	-HTRDY	-HTRDY	U2	TRDY		
6	-BPRI	-BPRI	-BPRI	U4	BPRI		
6	-BREQ0	-BREQ0	-BREQ0	C6	BREQ0		
6	-DEFER	-DEFER	-DEFER	U3	DEFER		
10	-IGNNE	-IGNNE	-IGNNE	AC13	IGNNE		
			TP24 -RSP	Y1	RSP		
			PICCLK	AA18	PICCLK		
			PICD0	AB21	PICD0		
			PICD1	Y20	PICD1		
6	-RS[0..2]	-RS[0..2]	-RS0	U1	RS0		
			-RS1	AA2	RS1		
			-RS2	W1	RS2		
			-SLEEP	AB12	SLEEP		
10	-SMI	-SMI	-SMI	AB10	SMI		
10	INTR	INTR	INTR	AB18	INTR	/ LINT0	
10,17	NMI	NMI	NMI	AC19	NMI	/ LINT1	
			BSEL0	AA12	BSEL0		
			GND	AB15	BSEL1		
10	-INIT	-INIT	-INIT	AA10	INIT		
6	-CPURST	-CPURST	-CPURST	A6	RESET		
17	HPWRGOOD	HPWRGOOD	HPWRGOOD	V5	PWRGOOD		
			-PREQ	AB20	PREQ		
			TMS	AD14	TMS		
			TDI	AD13	TDI		
			-TRST	AA14	TRST		
			TCLK	AA11	TCLK		

RN1H 1.5K, RN1E 1.5K, RN1F 1.5K, R2 270, RN1C 1.5K, R3 56.2, RN1D 1.5K, RN1B 1.5K, R4 680 — VTT
RN3B 1K, RN3A 1K, RN3C 1K — GND
RN4A 1.5K, RN4B 1.5K, RN4H 1.5K — VTT
RN3D 1K, RN3E 1K, RN3F 1K, RN4C 1.5K — GND, VTT

			EXF0 /	A3	L3	-A3	-A[3..31] 6
			EXF1 /	A4	K3	-A4	
			EXF2 /	A5	J2	-A5	
			EXF3 /	A6	L4	-A6	
			EXF4 /	A7	L1	-A7	
			BE0 /	A8	K5	-A8	
			BE1 /	A9	K1	-A9	
			BE2 /	A10	J1	-A10	
			BE3 /	A11	J3	-A11	
			BE4 /	A12	K4	-A12	
			BE5 /	A13	G1	-A13	
			BE6 /	A14	H1	-A14	
			BE7 /	A15	E4	-A15	
			DID0 /	A16	F1	-A16	
			DID1 /	A17	F4	-A17	
			DID2 /	A18	F2	-A18	
			DID3 /	A19	E1	-A19	
			DID4 /	A20	C4	-A20	
			DID5 /	A21	D3	-A21	
			DID6 /	A22	D1	-A22	
			DID7 /	A23	E2	-A23	
			ATTR0 /	A24	D5	-A24	
			ATTR1 /	A25	D4	-A25	
			ATTR2 /	A26	C3	-A26	
			ATTR3 /	A27	C1	-A27	
			ATTR4 /	A28	B3	-A28	
			ATTR5 /	A29	A3	-A29	
			ATTR6 /	A30	B2	-A30	
			ATTR7 /	A31	C2	-A31	
				A32	A4	-A32 TP1	
				A33	A5	-A33 TP2	
				A34	B4	-A34 TP3	
				A35	C5	-A35 TP4	
			AP0		AB1	-AP0 TP5	
			AP1		Y2	-AP1 TP6	
			AERR		AA1	-AERR TP7	
			BERR		E6	-BERR TP8	
			IERR		AD9	-IERR TP9	
			REQ0		T2	-HREQ0	-HREQ[0..4] -HREQ[0..4] 6
			REQ1		V4	-HREQ1	
			REQ2		V2	-HREQ2	
			REQ3		W3	-HREQ3	
			REQ4		W5	-HREQ4	
			RP		W2	-RP TP10	
			BPM0		W21	-BPM0 TP11	
			BPM1		W19	-BPM1 TP12	
			BP2		AA21	-BP2 TP13	
			BP3		Y21	-BP3 TP14	
			BINIT		V21	-BINIT TP15	
			ADS		AB2	-ADS	-ADS 6
			BNR		T4	-BNR	-BNR 6
			HIT		V1	-HIT	-HIT 6
			HITM		Y4	-HITM	-HITM 6
			DRDY		T1	-DRDY	-DRDY 6
			DBSY		AA3	-DBSY	-DBSY 6
			FERR		AC12	-HFERR	-FERR -FERR 10
			PRDY		W20	-PRDY	
			TDO		AC15	TDO TP25	

Q1 MMBT3904 (FERRB)
RN1G 1.5K — VTT
R1 1K
RN2A 10K — +3.3V
R5 56.2 — VTT

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Title	CPU	
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U1B

VCORE

Height = .100

H8 H10 H12 H14 H16 J7 J9 J11 J13 J15 K8 K10 K12 K14 K16 L7 L9 L11 L13 L15 M8 M10 M12 M14 M16 N7 N9 N11 N13 N15 P8 P10 P12 P14 P16 R7 R9 R11 R13 R15 T8 T10 T12 T14 T16 U7 U9 U11 U13 U15 — VCC

Set GTL voltage reference to 2/3 VTT or 1V

75 1%

VTT — R6 — GTLVREF — R7 150 1%

E5 E16 E17 F5 F17 U5 Y17 Y18 — VREF

Kemet C0603C104K4RAC 16V

C1 C2 C3 C4 C5 C6 C7 1uF

Provide some minimal series damping

L1 4.7uH 30mA — LPLL1 — R8 0 — PLL1 — L2 — PLL2

GND

C9 33uF 6V — T10 — PLL2 — M2

.1uF C8

1uF C10 1%

+2.5V — 1.5K R9 — 1.5K R10 1% — CLKREF — P2 — CLKREF

Clock reference = 1.25V

CMOS reference 1V

1.5K R11 — CMOSREF — AA9 — CMOSREF

1K R12 1% — AD18 — CMOSREF

110 R13 1% — EDGCTRLP — AA16 — EDGCTRLP

GND — 56.2 R14 1% — RTTIMPEDP — AD19 — RTTIMPEDP

VTT — 1.5K R15 — TESTHI1 — AD17 — TESTHI

1K 5 8 RN3G — TESTLO1 — Y5 — TESTLO1

1K 5 9 RN3H — TESTLO2 — N5 — TESTLO2

1uF C13

.1uF C14

TP42 TESTP1 AD20 — TESTP

TP45 TESTP2 H4 — TESTP

TP48 TESTP3 AA17 — TESTP

TP51 TESTP4 G4 — TESTP

Celeron these are NC

VCORE test points

G6 G7 G8 G9 G10 G11 G12 G13 G14 G15 G16 G17 H6 H17 J6 J17 K6 K17 L6 L17 M6 M17 N6 N17 P6 P17 R6 R17 T6 T17 U6 U17 V6 V7 V8 V9 V10 V11 V12 V13 V14 V15 V16 V17 W6 W7 W8 W9 W10 W11 W12 W13 W14 W15 W16 W17 Y6 Y7 Y8 AA6 AA7 AA8 AB6 AB7 AB8 AC6 AC7 AC8 AD6 AD7 AD8 — VCCT — VTT

(Celeron - VCC - see manual)

P1 — VCCT — VCORE

VID0 VID1 VID2 VID3 VID4 — VID[0..4] — VID[0..4] 16

(CATHODE) THERM - AB16 — THERM- — C12 2200pF

(ANODE) THERM + AA15 — THERM+

U2 Maxim MAX1617AMEE

DXN 4 — DXP 3 — STBY 15 — A0 10 — A1 9 — SDA 12 — SCL 14

VCC 2 — +3.3V

GND 7 — GND 8

ALERT 11 — -THERM — -THERM 10

GND .1uF C11

+3.3V

GND

8,10,13,17 SDA — SDA

8,10,13,17 SCL — SCL

U1C

Height = .100

A2 A7 A8 A12 A21 B1 B5 B6 B7 B8 B10 B15 B18 C9 C11 C15 C16 C19 D2 D6 D7 D9 E3 E7 E8 E9 E10 E11 E13 E19 F3 F6 F7 F8 F9 F10 F11 F12 F13 F14 F15 F16 F20 G3 G19 H2 H7 H9 H11 H13 H15 H20 J4 J8 J10 J12 J14 J16 J19 K2 K7 K9 K11 K13 K15 K20 L5 L8 L10 L12 L14 L16 L19 M7 M9 M11 M13 M15 M20 — GND

N2 N3 N4 N8 N10 N12 N14 N16 N18 N19 N20 P5 P7 P9 P11 P13 P15 P19 R3 R4 R5 R8 R10 R12 R14 R16 R20 T3 T5 T7 T9 T11 T13 T15 T18 T19 U8 U10 U12 U14 U16 U20 V3 V19 W4 W18 Y3 Y9 Y10 Y11 Y12 Y13 Y14 Y15 Y16 Y19 AA4 AA13 AA20 AB3 AB5 AB9 AB11 AB13 AB14 AB17 AC1 AC2 AC5 AC10 AC14 AC16 AC18 AC21 AD1 AD5 AD16 AD21 — GND

TP26 -GHI R2

TP27 RSVD2 AB19 — RSVD1 /-GHI, RSVD2

TP28 NC1 A15 — NC1

TP30 NC2 A16 — NC2

TP32 NC3 A17 — NC3

TP34 NC4 C14 — NC4

TP36 NC5 D8 — NC5

TP38 NC6 D14 — NC6

TP40 NC7 D16 — NC7

TP43 NC8 E15 — NC8

TP46 NC9 G2 — NC9

TP49 NC10 G5 — NC10

TP52 NC11 G18 — NC11

TP54 NC12 H3 — NC12

NC13 H5 NC13 — NC13 TP29

NC14 J5 NC14 — NC14 TP31

NC15 M4 NC15 — NC15 TP33

NC16 M5 NC16 — NC16 TP35

NC17 P3 NC17 — NC17 TP37

NC18 P4 NC18 — NC18 TP39

NC19 AA5 NC19 — NC19 TP41

NC20 AA19 NC20 — NC20 TP44

NC21 AC3 NC21 — NC21 TP47

NC22 AC17 NC22 — NC22 TP50

NC23 AC20 NC23 — NC23 TP53

NC24 AD15 NC24 — NC24 TP55

VCORE

Kemet C0805C105K8RAC X7R 10V 10%

C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C32 C33 C34 C35 C36 C37 C38 C39 1uF

Kemet C0603C104K4RAC 16V

C40 C41 C42 C43 C44 C45 C46 C47 C48 C49 C50 C51 C52 C53 C54 C55 C56 C57 C58 C59 C60 C61 1uF

VTT

Kemet C0805C105K8RAC X7R 10V 10%

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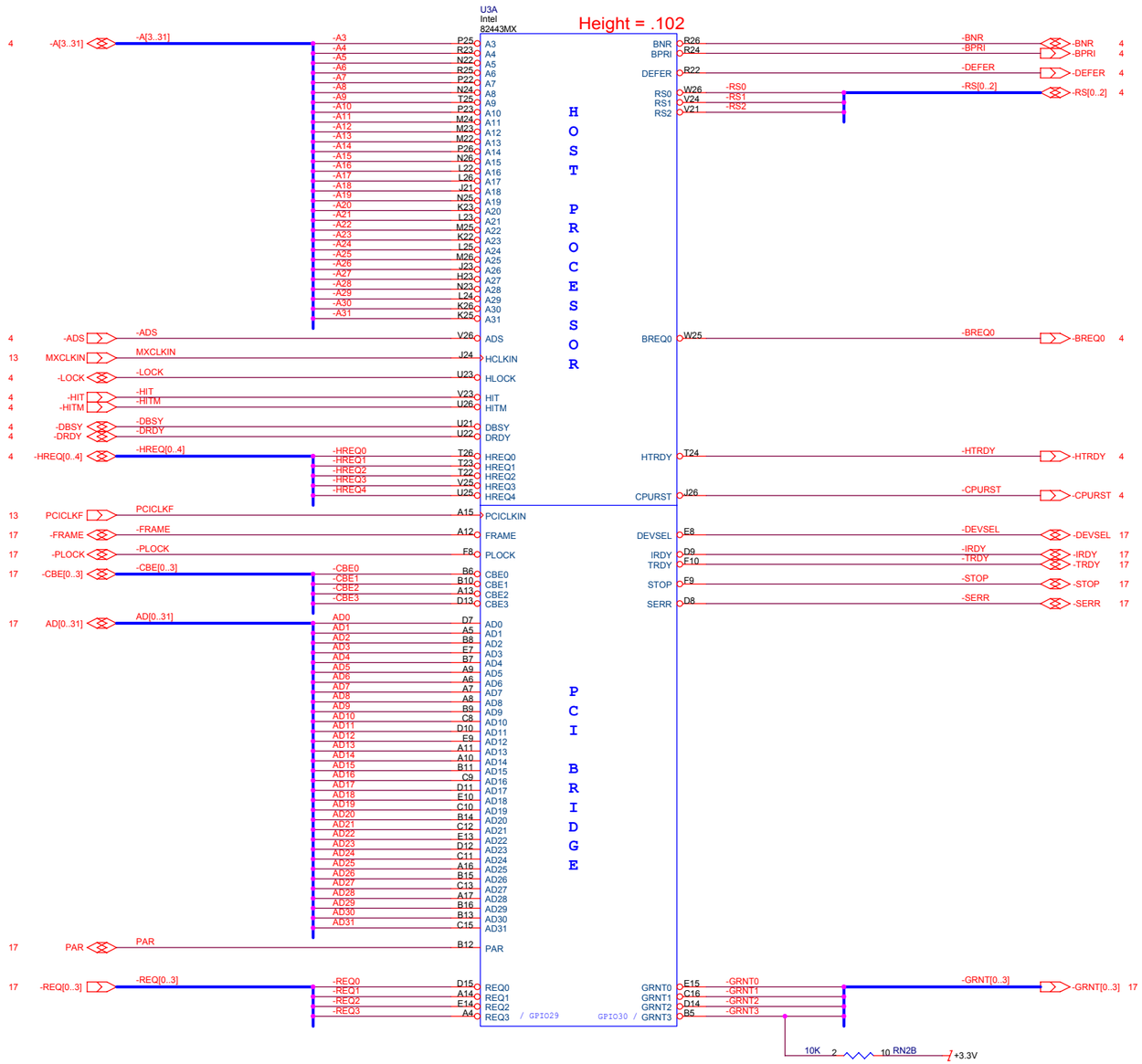

Title	440MX-CPU-PCI	
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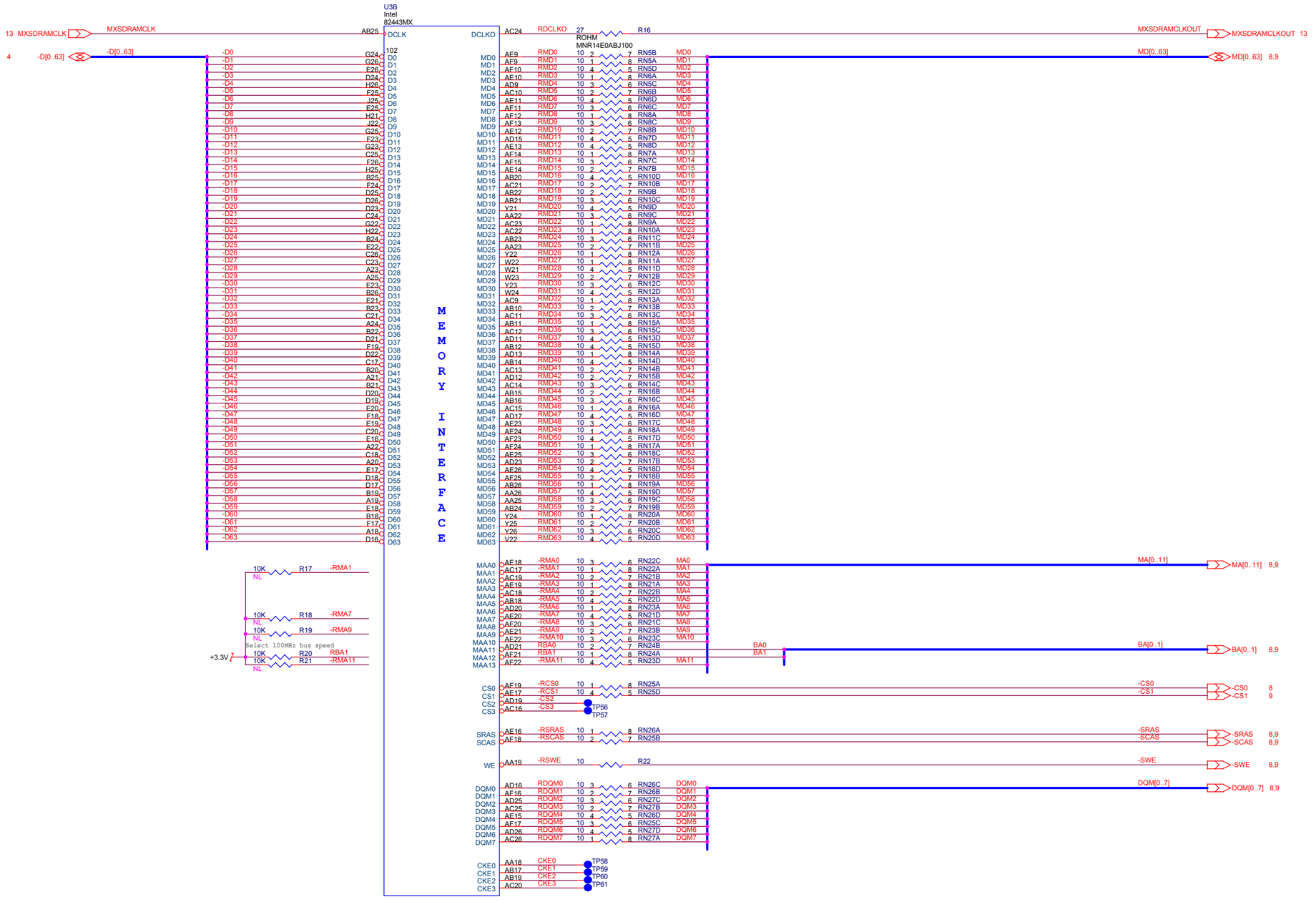

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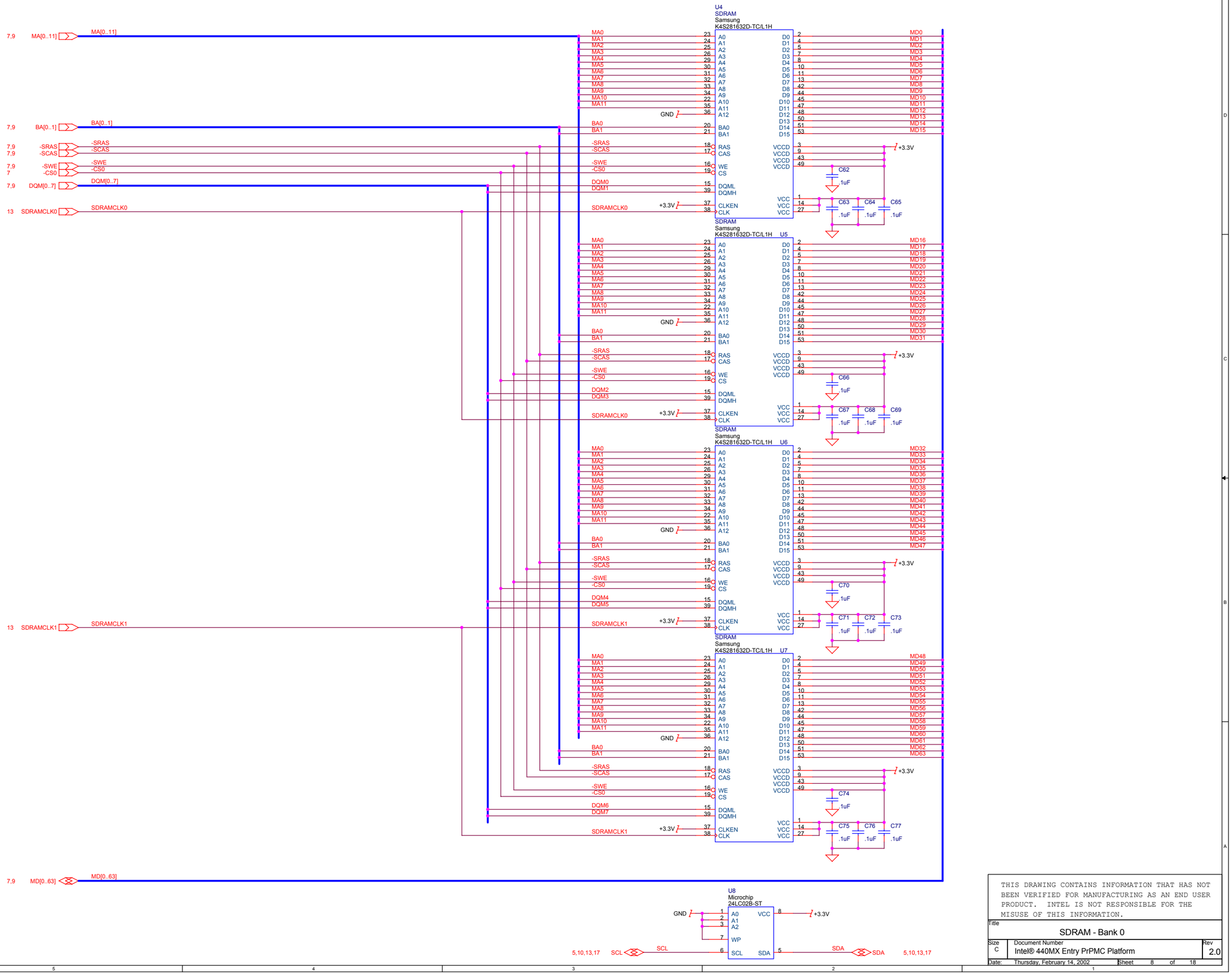

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Title: SDRAM - Bank 0

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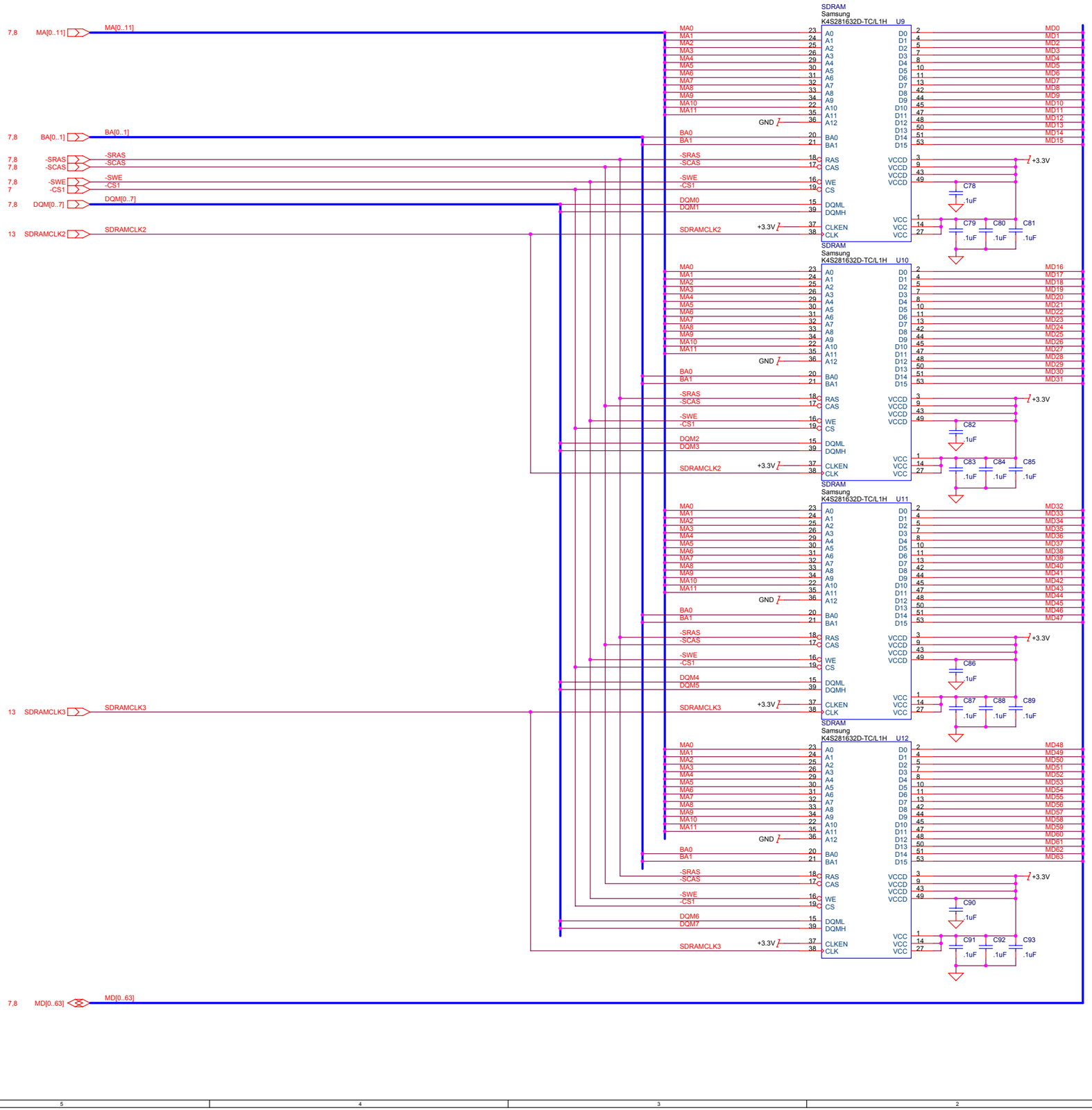

Title: SDRAM - Bank 1

Size	Document Number	Rev
C	Intel® 440MX Entry PrPMC Platform	2.0

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Height = .102

U3C

X-BUS + RTC + MISC CONTROL

SD[0..7] SD0 SD1 SD2 SD3 SD4 SD5 SD6 SD7

RN28E 10K RN28F 10K RN28D10K RN28G10K RN28C10K RN28B 10K RN28H10K RN28A10K

OSCMX OSC

IOCHRDY WS0 / GPIO21 IOCHRDY

-WS0 R23 2.2K

IRQ1 IRQ3 IRQ4 IRQ5 IRQ6 IRQ7 IRQ8 / GPIO06 IRQ12 IRQ14

RN2C RN2D RN2E RN2G RN2H RN31A RN31D RN31G RN31H RN32A

-IRQ8 IRQ12 IRQ14 R24 2.2K

SERIRQ SERIRQ / GPIO07

RN33H 4.7K

-INTA -INTB -INTC -INTD PCIRQA PCIRQB PCIRQC / GPIO22 PCIRQD / GPIO23

RN33A 4.7K RN33B 4.7K

DREQ[1..3] DREQ0 DREQ1 DREQ2 DREQ3 / GPIO27

RN33C 4.7K RN33D 4.7K RN32C 10K

-REQA REQA / GPIO02 R25 2.2K

-FERR FERR

A20GATE A20GATE

RN32F 10K GPIO11 BATLOW / GPIO11

RN32G 10K GPIO10 LID / GPIO10

-THERM RN32H 10K THERM / GPIO08

RN34A 10K GPIO12 RI / GPIO12

RN34B 10K GPIO0 PME / GPIO00

RN34C 10K GPIO24 EXTSMI / GPIO24

USBCLK USBOC0 USBOC1 AC97CLK AC97SDIN0 AC97SDIN1 AC97SYNC PWRGOOD -KBDRST

USBCLK OC0 OC1 AC97CLK AC97SDIN0 AC97SDIN1 AC97SYNC PWROK KBDRSTIN

-PWRBTN R32 2.2K RN34D 10K

PWRBTN

GPIO1 GPIO4 GPIO5 GPIO9 GPIO13 GPIO15 GPIO17 GPIO18 GPIO20

-BOOTWE RN35E 10K

-MXTEST R34 10K

TEST

RTCX1 RTCX2 1M R36 Y1 FOX 32.768KHz FST327 C94 22pF C95 22pF

R35 1K R37 1K PUROM3V -RBOOTWE

D1 SD103AW-13 Q2 MMBT3904 BOOTWE R38 10K

Q3 Vishay Si2306DS

Track width minimum of 24mil.

RN35F 10K RN35G 10K RN35H 10K

-BIOSCS -MEMRD -MEMWR

U14 Atmel AT49LV002T-12JC LD=PLCC32

SA[0..15] SD[0..7] VCC +3.3V

SOCKET BIOS Socket

Height = .140

Dual footprint these two devices. PLCC32 pin socket loaded for debug. Production uses TSOP.

U13 Atmel AT49LV002T-12TC NL=PLCC32

SA[0..15] SD[0..7] VCC +3.3V GND GND

-BIOSCS -MEMRD -MEMWR VPP CE OE WE RESET

SA0 SA1 SA2 SA3 SA4 SA5 SA6 SA7 SA8 SA9 SA10 SA11 SA12 SA13 SA14 SA15 SA16 SA17 SA18

MEMRD -MEMRD MEMWR -MEMWR IORD -IORD IOWR -IOWR SYSCLK SYSCLK TP62

CLKRUN -CLKRUN CPUSTP -CPUSTP PCISTP -PCISTP TP63 TP64

A20M -A20M SMI -SMI STPCLK -STPCLK R102 0 NL=NMI

NMI ~NMI INTR NMI INTR

DACK0 DACK1 DACK2 DACK3 -DACK0 -DACK1 -DACK2 -DACK3 TP65 -DACK[1..3]

TC TC

GRNTA -GRNTA RN32D 10K

IGNNE -IGNNE

SUSCLK SUSTAT SUSCLK -SUSTAT TP66 RN32E 10K +3.3V

SUSA SUSB SUSC -SUSA -SUSB -SUSC TP67 TP68 TP69

BIOSCS KBDCS MCCS -BIOSCS -KBDCS -MCCS TP70 TP71

PCS0 PCS1 -PCS0 -PCS1 TP72 TP73

SMBCLK SMBDATA SCL SDA

SPKR -SPKR TP74

USBP0- USBP0+ USBP1- USBP1+ RUSBP0- RUSBP0+ RUSBP1- RUSBP1+ R26 33 R27 33 R28 33 R29 33

R30 4.7K R31 4.7K +3.3V

AC97SDOUT AC97RST -AC97RST

RSTDRV PCIRST INIT RSTDRV -PCIRST -INIT

GPIO1 GPIO4 GPIO5 GPIO9 GPIO13 GPIO15 GPIO17 GPIO18 R33 2.2K RN34E RN34F RN34G RN34H RN35A RN35B RN35C RN35D +3.3V

SA[0..15] SA0 SA1 SA2 SA3 SA4 SA5 SA6 SA7 SA8 SA9 SA10 SA11 SA12 SA13 SA14 SA15 SA16 SA17 SA18 RN29B 10K RN29C 10K RN29F 10K RN29E 10K RN29D 10K RN29A 10K RN29H 10K RN29G 10K RN30A 10K RN30B 10K RN30C 10K RN30D 10K RN30E 10K RN30F 10K RN30G 10K RN30H 10K RN2F 10K +3.3V

MEMRD MEMWR RN31B 10K RN31E 10K RN31C 10K RN31F 10K

IORD IOWR -IORD -IOWR

-A20M SMI STPCLK -SMI -STPCLK

RN32B 10K

NMI INTR NMI INTR

-DACK[1..3] TC -IGNNE

SCL SDA

AC97SDOUT -AC97RST RSTDRV -PCIRST -INIT

Title	440MX-XBus	
Size C	Document Number Intel® 440MX Entry PrPMC Platform	Rev 2.0
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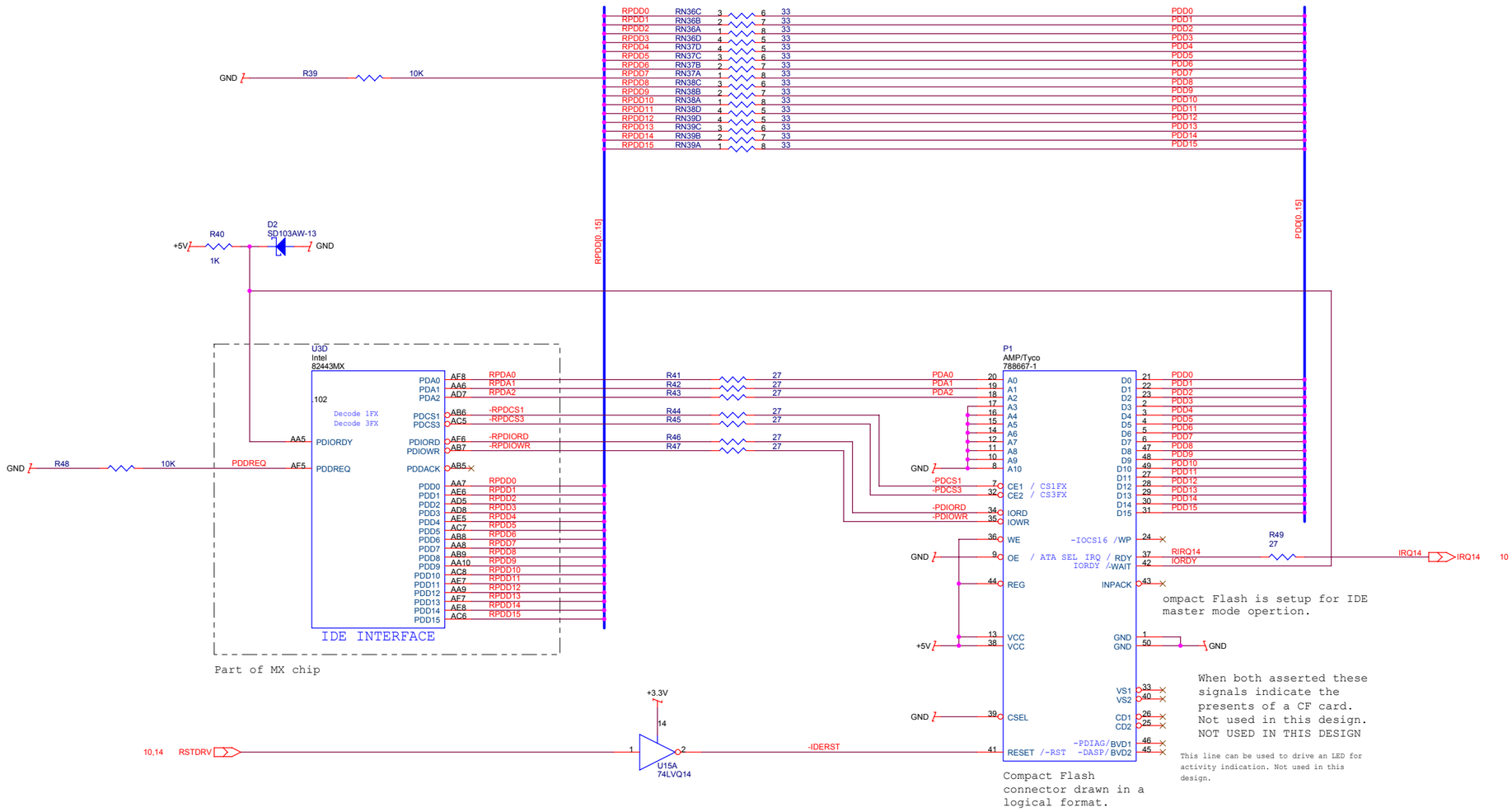
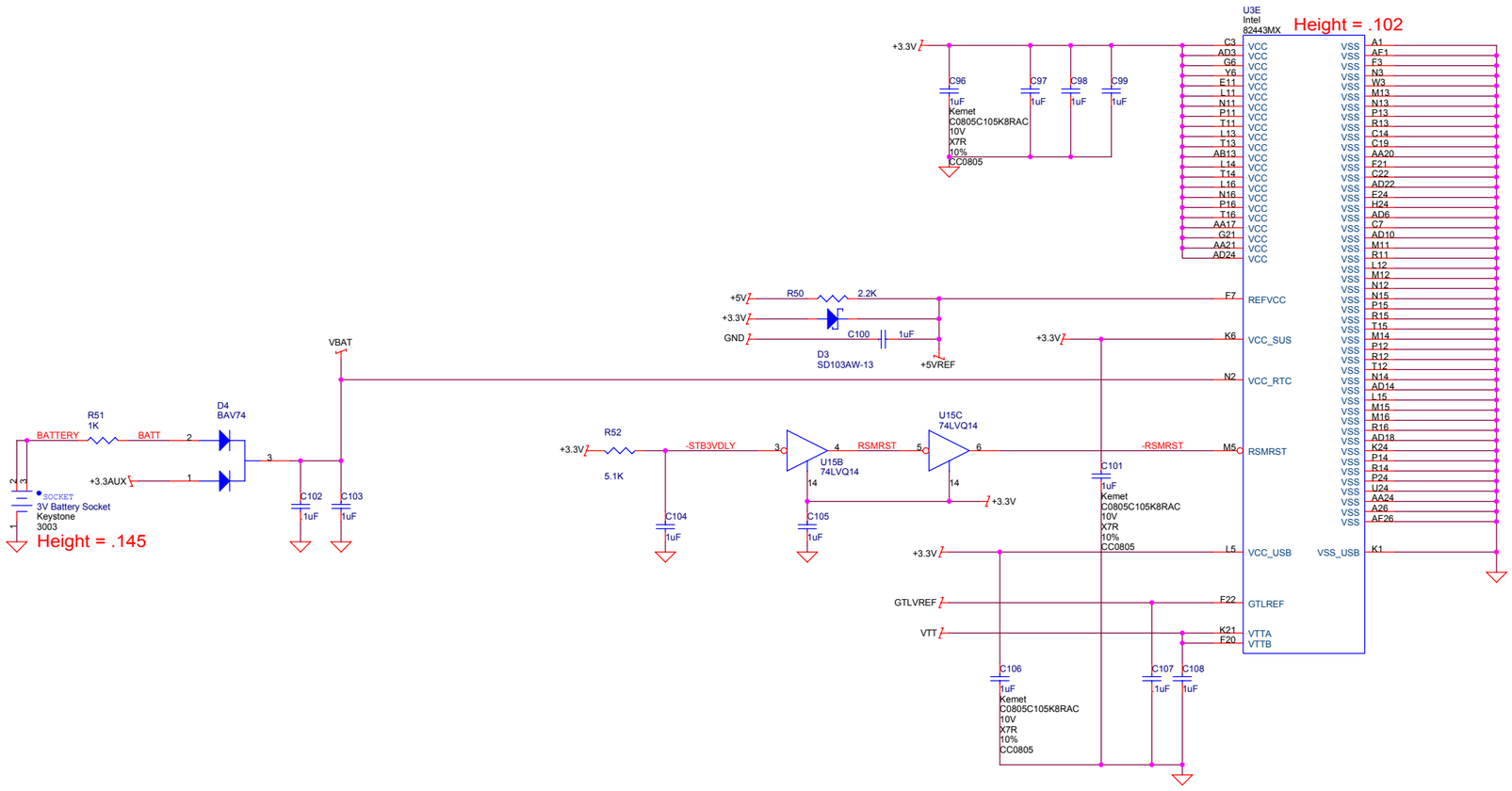


Title	440MX-IDE	
Size: C	Document Number: Intel® 440MX Entry PrPMC Platform	Rev: 2.0
Date: Thursday, February 21, 2002	Sheet 11 of 18	



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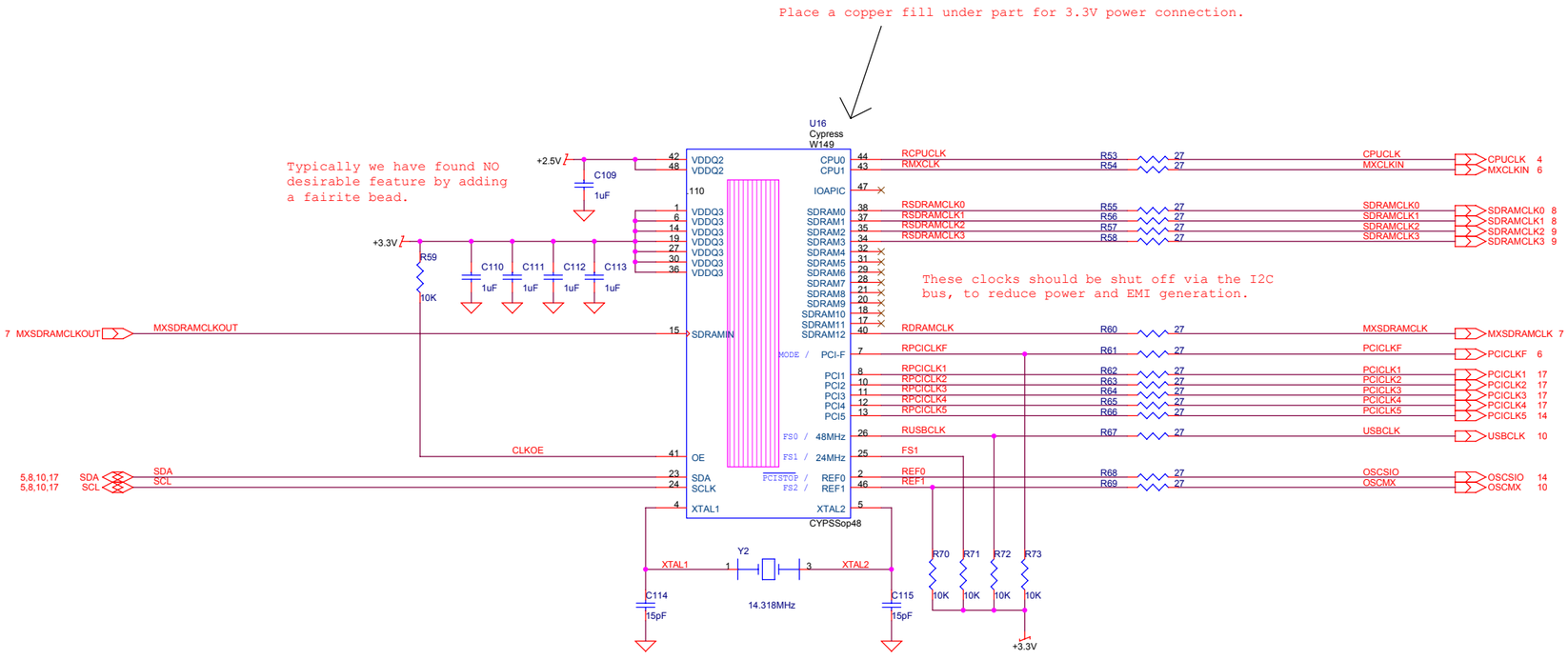
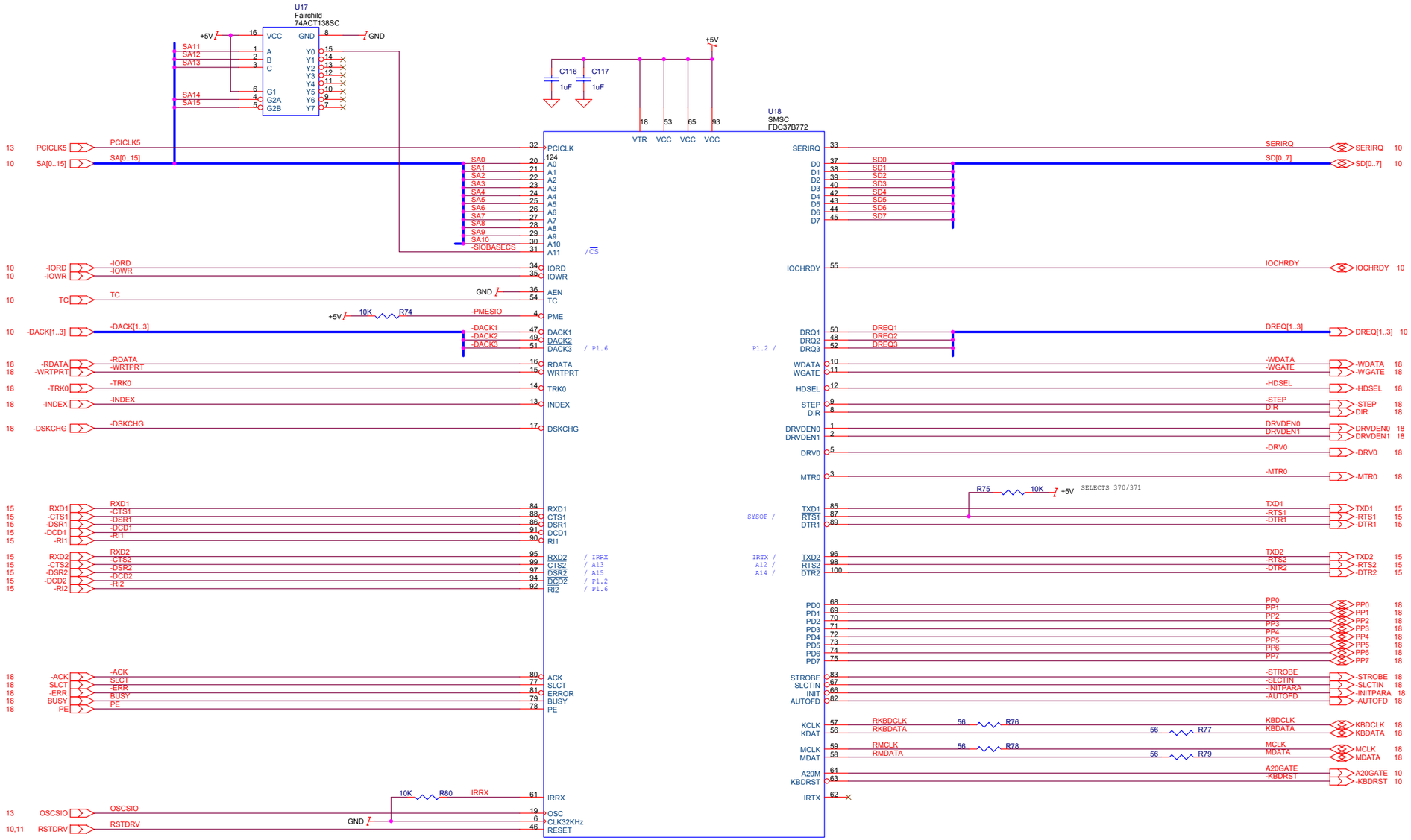
Title	440MX Power	
Size: C	Document Number: Intel® 440MX Entry PrPMC Platform	Rev: A1
Date: Thursday, February 21, 2002	Sheet 12 of 18	



THIS DRAWING CONTAINS INFORMATION THAT HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Title: Clocking		
Size: C	Document Number: Intel® 440MX Entry PrPMC Platform	Rev: 2.0
Date: Thursday, February 21, 2002	Sheet 13 of 18	



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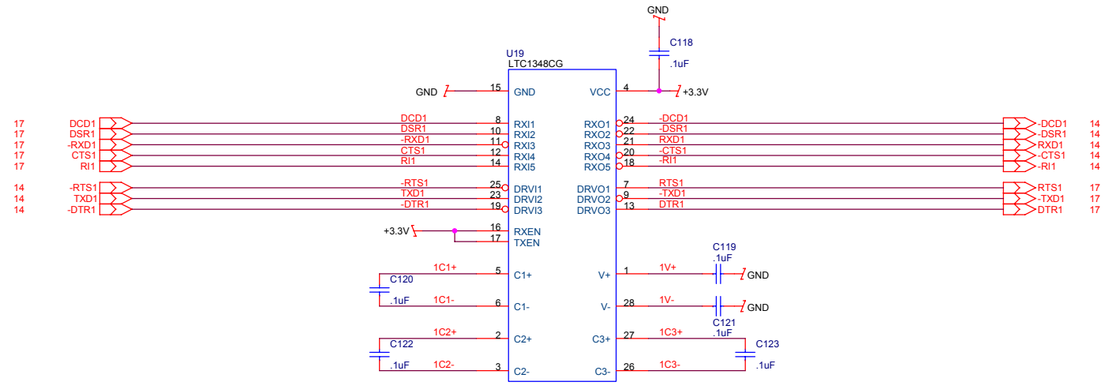
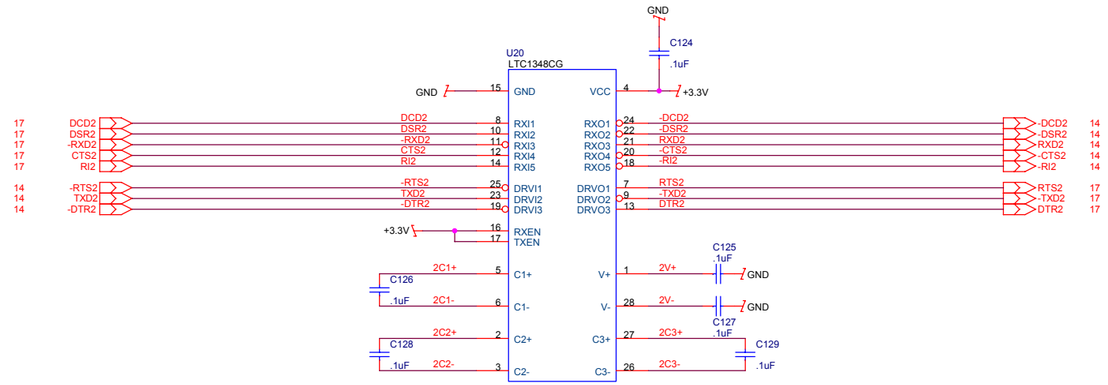
Title	SuperIO	
Size: C	Document Number: Intel® 440MX Entry PrPMC Platform	Rev: 2.0
Date: Thursday, February 21, 2002	Sheet 14 of 18	





Title: Serial Buffers

Size: C | Document Number: Intel® 440MX Entry PrPMC Platform | Rev: 2.0

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VID4	VID3	VID2	VID1	VID0	VOUT
1	1	1	1	0	0.925V
1	1	1	0	1	0.950V
1	1	1	0	0	0.975V
1	1	0	1	1	1.000V
1	1	0	1	0	1.025V
1	1	0	0	1	1.050V
1	1	0	0	0	1.075V
1	0	1	1	1	1.100V
1	0	1	1	0	1.125V
1	0	1	0	1	1.150V
1	0	1	0	0	1.175V
1	0	0	1	1	1.200V
1	0	0	1	0	1.225V
1	0	0	0	1	1.250V
1	0	0	0	0	1.275V
0	1	1	1	1	1.30V
0	1	1	1	0	1.35V
0	1	1	0	1	1.40V
0	1	1	0	0	1.45V
0	1	0	1	1	1.50V
0	1	0	1	0	1.55V
0	1	0	0	1	1.60V
0	1	0	0	0	1.65V
0	0	1	1	1	1.70V
0	0	1	1	0	1.75V
0	0	1	0	1	1.80V
0	0	1	0	0	1.85V
0	0	0	1	1	1.90V
0	0	0	1	0	1.95V
0	0	0	0	1	2.00V
0	0	0	0	0	2.05V

+5V
GND
C130 330uF 10V Vishay 592D337X0010W2T
C131 330uF 10V Vishay 592D337X0010W2T
C132 1uF Kemet C0805C105K8RAC 10V CC0805
C133 330uF 10V Vishay 592D337X0010W2T
C134 330uF 10V Vishay 592D337X0010W2T
Allows maximum current adjustment
R81 1K NL
R82 0 Dale CRCW0603000RT1
R83 10
U21 Maxim MAX1711 MAXQSOP24
V+ VDD VCC BST DH LX ILIM TON D0 D1 D2 D3 D4 SHDN SKIP REF CC PGND FB FBS GNDS PGOOD GND
D5 Diodes Inc. SD103AW SOD123
R5V
C135 .1uF
ILIM
TON
BST
DH
R84 10
DHR
U22 Vishay Si4800DY
C136 .1uF
Dale CRCW0603000RT1
Set switcher freq=550KHz
GND
R85 0 NOT LOADED=300KHz
5 VID[0..4]
VID0 VID1 VID2 VID3 VID4
+5V
R86 1K Dale CRCW0603102JRT1
-SHDN
REF
C142 22uF Kemet C0805C224K3RAC
CC
C143 470pF
C144 470pF NL
DL
DLR
R87 10
DL1
U23 Vishay Si4812DY
DL2
U24 Vishay Si4812DY
R88 10
Height = .224
L2 2.0uH 30% 10.7A .0033 Ohms Panasonic ETQP6F2R0H
VCORE
C137 150uF 4V Kemet A700D157M004AT Height = .122
C138 150uF 4V Kemet A700D157M004AT Height = .122
C139 150uF 4V Kemet A700D157M004AT Height = .122
C140 150uF 4V Kemet A700D157M004AT Height = .122
C141 150uF 4V Kemet A700D157M004AT Height = .122
GNDS
R89 1K Dale CRCW0603102JRT1
VRMPWRGD
VRMPWRGD 17
R90 1K Dale CRCW0603102JRT1
+3.3V

Micrel 2.5V @ 1A
Max. PD=.8W
+3.3V
+2.5V
U25 Micrel MIC39100-2.5BS SOT223H71
VIN GND VOUT TAB
C145 1uF Kemet C0805C105K8RAC 10V CC0805
C146 1uF Kemet C0805C105K8RAC 10V CC0805

Linear Technology 1.5V @ 4A
Max. PD=7.2W
+1.5V
VTT
Height = .180
U26 Linear Technology LT1585ACM-1.5
VIN GND VOUT TAB
C147 1uF Kemet C0805C105K8RAC 10V CC0805
C148 330uF 10V Vishay 592D337X0010W2T
C149 330uF 10V Vishay 592D337X0010W2T Height = .079

ONE INCH OF COPPER PAD NEEDED FOR HEAT SINK RELEAF. ALSO TRY TO PLACE IN OPEN CONNECTOR AREA

Title: Voltage Regulator
Size: C
Document Number: Intel® 440MX Entry PrPMC Platform
Rev: 2.0
Date: Thursday, February 14, 2002

PCI BUS

Tyco/AMP 120527-1 — JN1 PMC-Jn1

1	TCK	2	-12V
3	GND	4	INTA
5	INTB	6	INTC
7	PRESENT	8	+5V
9	INTD	10	PCI-RSVD1
11	GND	12	+3.3AUX
13	PCICLK	14	GND
15	GND	16	GRNT
17	REQ	18	+5V
19	VIO	20	AD31
21	AD28	22	AD27
23	AD25	24	GND
25	GND	26	CBE3
27	AD22	28	AD21
29	AD19	30	+5V
31	VIO	32	AD17
33	FRAME	34	GND
35	GND	36	IRDY
37	DEVSEL	38	+5V
39	GND	40	LOCK
41	SDONE	42	SBO
43	PAR	44	GND
45	VIO	46	AD15
47	AD12	48	AD11
49	AD9	50	+5V
51	GND	52	CBE0
53	AD6	54	AD5
55	AD4	56	GND
57	VIO	58	AD3
59	AD2	60	AD1
61	AD0	62	+5V
63	GND	64	REQ64

Tyco/AMP 120527-1 — JN2 PMC-Jn2

1	+12V	2	TRST
3	TMS	4	TDO
5	TDI	6	GND
7	GND	8	PCI-RSVD2
9	PCI-RSVD1	10	PCI-RSVD3
11	PULLUP	12	+3.3V
13	RESET	14	PULLDWN1
15	+3.3V	16	PULLDWN2
17	PME	18	GND
19	AD30	20	AD29
21	GND	22	AD26
23	AD24	24	+3.3V
25	IDSEL	26	AD23
27	+3.3V	28	AD20
29	AD18	30	GND
31	AD16	32	CBE2
33	GND	34	IDSELB
35	TRDY	36	+3.3V
37	GND	38	STOP
39	PERR	40	GND
41	+3.3V	42	SERR
43	CBE1	44	GND
45	AD14	46	AD13
47	M66EN	48	AD10
49	AD8	50	+3.3V
51	AD7	52	PMC-RSVD3
53	+3.3V	54	PMC-RSVD4
55	PMC-RSVD1	56	GND
57	PMC-RSVD2	58	EREADY
59	GND	60	RESETOUT
61	ACK64	62	+3.3V
63	GND	64	MONARCH

Tyco/AMP 120527-1 — JN4 PMC-Jn4

1	REQ3	2	+3.3V
3	REQ2	4	GRNT3
5	GND	6	GRNT2
7	REQ1	8	+3.3V
9	REQ0	10	GRNT1
11	GND	12	GRNT0
13	PCICLK1	14	GND
15	GND	16	PCICLK2
17	PCICLK3	18	GND
19	GND	20	PCICLK4
21	PWRGOOD	22	GND
23	NMI	24	SYSRST
25	SCL	26	SDA
27	GND	28	+5V
29	GPIO0	30	GPIO4
31	GPIO1	32	GPIO5
33	GPIO2	34	GPIO6
35	GPIO3	36	GPIO7
37	GND	38	+5V
39	USBOC0	40	USBOC1
41	USBP0+	42	USBP1+
43	USBP0-	44	USBP1-
45	GND	46	+5V
47	DCD1	48	DCD2
49	RXD1	50	-RXD2
51	TXD1	52	-TXD2
53	DTR1	54	DTR2
55	DSR1	56	DSR2
57	RTS1	58	RTS2
59	CTS1	60	CTS2
61	RI1	62	RI2
63	GND	64	+5V

PCI BUS ADDITIONS

Title: PMC Connectors

Size: C | Document Number: Intel® 440MX Entry PrPMC Platform | Rev: 2.0

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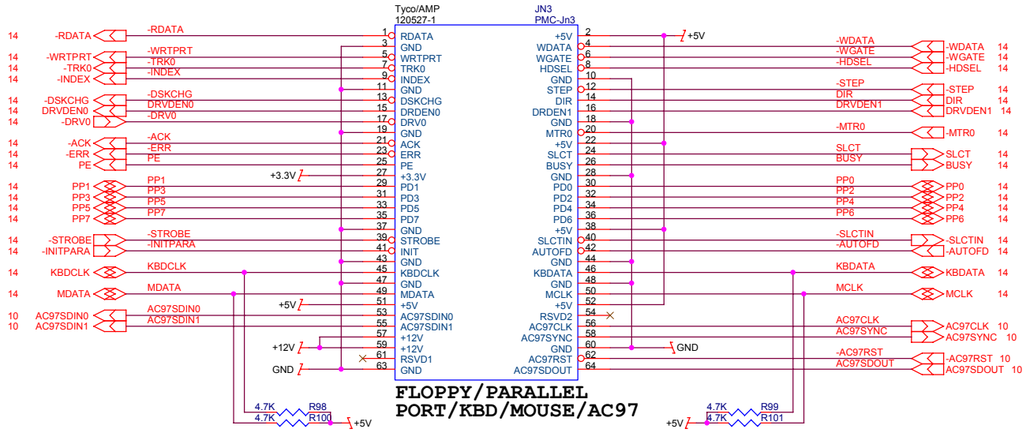

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Title: PMC Debug Connector		
Size: C	Document Number: Intel® 440MX Entry PrPMC Platform	Rev: 2.0
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